

February 11, 2004

To: Commissioner for Patents

P.O.Box 1450

Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572

28 Davis Avenue

Poughkeepsie, N.Y. 12603

Subject:

Serial No. 10/718,876 11/21/03

Li-Te S. Lin et al.

PHOSPHORIC ACID FREE PROCESS FOR POLYSILICON GATE DEFINITION

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation
In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on February , 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date Stopher Backer 2/12/04

- U.S. Patent 6,579,809 to Yang et al., "In-situ Gate Etch Process for Fabrication of a Narrow Gate Transistor Structure with a High-k Gate Dielectric," discusses a method of small geometry gate formation of the surface of a high-k gate dielectric.
- U.S. Patent 6,403,432 to Yu et al., "Hardmask for a Salicide Gate Process with Trench Isolation," describes a method for forming a self-aligned polysilicon gate MOSFET with silicon oxide shallow trench isolation.
- U.S. Patent 6,524,938 to Tao et al., "Method for Gate Formation with Improved Spacer Profile Control," discloses a process for the creation of an improved gate spacer profile.
- U.S. Patent 6,251,719 to Wang, "Poly Gate Process that Provides a Novel Solution to Fix Poly-2 Residue Under Poly-1 Oxide for Charge Coupled Devices," discloses a method for the creation of poly gate electrodes.
- U.S. Patent 5,612,249 to Sun et al., "Post-gate LOCOS," discloses a method of defining a local oxidation of silicon (LOCOS) field isolation process after a poly gate is deposited.

- U.S. Patent 6,283,131 to Chen et al., "In-situ Strip

 Process for Polysilicon Etching in Deep Submicron Technology,"

 discusses a method of patterning the polysilicon layer in the

 manufacture of an integrated circuit device.
- U.S. Patent 6,531,350 to Satoh et al., "Twin MONOS Cell Fabrication Method and Array Organization," discusses a fabricating method and its array organization for a high-density twin MONOS memory device integrating a twin MONOS memory cell array and CMOS logic device circuit.

Sincerely,

Stephen B. Ackerman,

Reg. No. 37761

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EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.